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(54) Title: **OVERLAY METROLOGY MARK**

(57) **Abstract:** An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with and in particular developed on a first layer and a second mark portion associated with and in particular developed on the surface of a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal array of individual test structures. A method of marking and a method of determining overlay error are also described.

**WO 2004/090978 A2**

### **Overlay Metrology Mark**

The invention relates to overlay metrology during semiconductor device  
5 fabrication, and in particular to an overlay alignment mark to facilitate  
alignment and/or measure the alignment error of two layers on an integrated  
circuit structure during its fabrication.

Modern semiconductor devices, such as integrated circuits, are typically  
10 fabricated from wafers of semiconductor material. In particular, a wafer is  
fabricated comprising a succession of patterned layers of semiconductor  
material.

Circuit patterns are fabricated using a variety of long established techniques,  
15 for example making use of lithographic techniques. Precise positioning and  
alignment during fabrication is of great significance in the manufacture of  
accurate patterns. For example, alignment control of the exposure tool is  
important in ensuring a consistent process. Alignment methodologies are  
established in this regard, in which statistical and modelling techniques are  
20 used to determine the alignment of a reticle with a pattern created by or in  
association with the exposure tool to facilitate alignment of the exposure tool.  
The technique typically exploits images generated within the exposure tool  
optics, or projected onto the wafer by the exposure tool optics. Similar model-  
based and statistical methods have been employed to align for example an  
25 exposure tool during pattern fabrication.

Although such alignment technology has an established utility, and is  
important in device fabrication, it relates to alignment of fabrication tooling  
only. This can be a limitation in relation to semiconductor structures  
30 comprised of a succession of pattern layers of semiconductor material where it

is desirable in relation to such wafers to provide a methodology enabling a determination of the misregistration between fabricated layers themselves.

Overlay metrology in semiconductor device fabrication is used to determine how well one printed layer is overlaid on a previously printed layer. Close alignment of each layer at all points within the device is crucial for reaching the design goals and hence the required quality and performance of the manufactured device. It is consequently of importance for the efficiency of the manufacturing process that any alignment error between two patterned layers on a wafer, especially successive patterned layers can be measured quickly and accurately. It is similarly important to be able to measure any alignment error between successive exposures in the same layer, and where reference is made herein for convenience to two layers it will be understood where appropriate to apply equally to two exposures in the same layer.

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Misregistration between layers is referred to as overlay error. Overlay metrology tools are used to measure the overlay error. This information may be fed into a closed loop system to correct the overlay error.

20 Current overlay metrology employs optically readable target patterns, printed onto the successive layers of a semiconductor wafer during fabrication. The relative displacement of two successive layers is measured by imaging the patterns at high magnification, digitizing the images, and processing the image data using various known image analysis algorithms to quantify the overlay error. Overlay metrology techniques thus involve the direct measurement of misregistration between patterns provided in direct association with each of the fabricated layers under investigation. In particular, patterns are developed in or on the surface of each of the layers, or may be latent images, rather than images generated within or projected from the optics of an imaging instrument.

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The pattern of the target mark may be applied to the wafer by any suitable method. In particular, it is often preferred that the mark is printed onto the wafer layers for example using photolithographic methods. Typically, the same technique is used to apply overlay target marks on each of two wafer layers to be tested to enable alignment information to be measured which is representative of the alignment of the layers. Accuracy of layer alignment should correspond to accuracy of circuit pattern alignment within the fabricated wafer.

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Current overlay metrology is normally practised by printing targets with rectangular symmetry. For each measurement two targets are printed, one in the current layer and one in a previous layer, or one in association with each pattern in a common layer. The choice of which previous layer to use is determined by process tolerances. The two targets have a nominally common centre, but are printed with different sizes so that they can be differentiated. Normally, but not always, the target printed in the current layer is the smaller of the two targets. An overlay measurement in such a system is the actual measured displacement of the centres of the two targets.

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Current preferred practice is that the size of the targets is designed such that both can be imaged simultaneously by a bright-field microscope. Imaging considerations determine that the larger of the two targets is typically a 25µm square on the outside. This arrangement permits capture of all of the necessary data for the performance of the measurement from a single image. Measurements at a rate of one in every two seconds or less are possible using current technology.

The procedure necessarily requires that the target and its image are symmetric, since otherwise there is no uniquely defined centre point. Without symmetry

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there is an uncertainty in the measurement, which may be more than can be tolerated. Within that general requirement, optimal sizes and shapes of current designs of targets to be measured are well known. The targets are positioned in the scribe area at the edge of the fabricated circuit.

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It is generally desirable that the measurement targets maintain axial symmetry about the optical axis of the measurement tool, since accurate measurement requires very close control of image aberrations. To achieve this it can also therefore be advantageous to use marks at or with symmetry centred about the

10 system axis.

Marks exhibiting symmetry are usually aligned in a known and consistent relationship relative to the crystal lattice of the wafer. Where this defines "X" and "Y" directions these are conveniently used as reference directions for the

15 imaging apparatus. The "X" and "Y" planes are more specifically relevant to the wafer than they are to the optics, but it is normal to choose to align the wafer such that "X" corresponds to the horizontal and "Y" to the vertical as viewed through the microscope. It is possible in principle to measure at any other orientation, but for many mark symmetries advantages are conferred if

20 the marks are arranged to have symmetry about what are conventionally termed the "X" and the "Y" axes, which allows the optimum performance to be obtained from the metrology apparatus.

In most prior art systems, measurements are therefore made from the targets

25 by computing a centre line for each different target. The overlay measurement is the difference in the centre lines. Most of the target designs in general use permit measurement of the vertical and horizontal overlay displacement from a single image.

Measurement errors must be controlled to a very small amount. Errors known to arise are classified as random errors, characterized by determination of measurement precision; and systematic errors, characterized by tool induced errors, tool-to-tool measurement differences and errors introduced by asymmetry in the targets being measured. Successful application of overlay metrology to semiconductor process control is generally held to require that, combined, these errors are less than 10% of the process control budget. This measurement error budget is in practice in the range 1 to 5 nm, and will remain so in the foreseeable future.

10

Measurement precision is easily determined by analysis of the variations of repeated measurements. Different forms of precision may be determined by well known appropriate methods, allowing determination of the static, short-term and long-term components of precision.

15

Determining the contribution of the measurement tool alone to errors is achieved by comparing measurements made with the target in its normal presentation with a measurement made after rotating the target by 180° with respect to the imaging system. Ideally the measurement will simply change sign. The average of the measurements at 0° and 180° is called *Tool Induced Shift* (TIS), as is well known to those skilled in the art, and is widely accepted as a measure of the tool's systematic error contribution. Measurements of TIS differ from tool to tool and with process layer. Subtraction of the estimated TIS error from the measurements allows removal of the TIS error from the measurements, but at the expense of the additional time taken to measure the target twice.

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Different tools, even when of the same type, will make slightly different measurements, even after allowing for precision and TIS errors. The

magnitude of this error can be determined experimentally by comparing the averages of repeated measurements at 0° and 180° on two or more tools.

The contributions of precision, TIS and tool-to-tool differences are normally combined through a root-sum-square product, or alternative appropriate method, to determine the total measurement uncertainty due to the measurement process. The total measurement uncertainty must be less than 10% of the overall overlay budget for the process if the metrology is to have value. Existing measurement tools and procedures achieve a total uncertainty within that required for current process technologies but insufficient for future requirements.

By contrast, although the contribution of asymmetry in the measurement target itself is widely understood it is not normally determined. It is known that in many cases it can be much larger than the tool contribution to measurement uncertainty. There are two sources of error to be considered:

1. Imperfection in the manufacture of the target which leads to an uncertainty in its location. An example of this is physical asymmetry of the target, caused perhaps by uneven deposition of a metal film.
2. Difference in the displacement of the two layers at the measurement target and the genuine overlay of the same layers in the device being manufactured. These can arise from errors in the design and manufacture of the reticles used to create the patterns on the wafer, proximity effects in the printing process and distortion of the films after printing by other process steps.

These measurement errors represent a practical limitation of the current state of the art which causes severe problems in the application of overlay metrology to semiconductor process control.

Improvements to the first of these problems can sometimes be achieved by fabricating the features in the measured targets from much smaller objects - lines or holes. The common term for this technique is "segmentation". These smaller features are printed at the design rule for the process, currently in the  
5 range 0.1-0.2  $\mu\text{m}$ , and are grouped close together. They are too small to be individually resolved by the optical microscopes used in overlay metrology tools. The small features are grouped into larger shapes in the pattern of traditional overlay targets. The use of small features avoids some of the mechanisms causing imperfections in the shape of the manufactured targets, in  
10 part by taking advantage of the optimization of the manufacturing process for objects of this size and shape.

A further problem is introduced by the size of the targets, which are a significant fraction of the space available in the scribe area surrounding the  
15 devices being fabricated. It is desired that the size of these areas be reduced, which means that it is also highly desirable that the measurement targets be made smaller. However, the size of the target cannot be reduced too much, since accurate measurement requires that the measured features are not smaller than the resolution of the microscope system, and achieving good precision  
20 requires that as many as possible of such features are visible in the image.

It has been shown (Smith, Nigel P.; Goelzer, Gary R.; Hanna, Michael; Troccolo, Patrick M., "*Minimizing overlay measurement errors*", August 1993, Proceedings of SPIE Volume: 1926 Integrated Circuit Metrology,  
25 Inspection, and Process Control VII, Editor(s): Postek, Michael T) that space must be left between the features printed from the two layers else the proximity of one to another causes an error in the measurement. The magnitude of this error depends on the resolution of the imaging microscope system, but must be 5  $\mu\text{m}$  or greater in practical designs if the measurement



error is to be contained within practical limits. This proximity effect further limits the extent to which the size of the targets can be reduced.

However, high speed is one of the key advantages of existing overlay metrology practice, and any process development must not lose this advantage if it is to be viable in production use. This requirement means that uncertainty reduction by the use of repeated measurements is highly undesirable. There is thus a general desire to develop alternative overlay patterns and/or analysis methods which apply the basic principles of existing metrologies but in a manner that mitigates some or all of these errors to produce an improved fabrication metrology, and in particular a metrology offering improved accuracy without substantial loss of throughput speed.

In accordance with the present invention in a first aspect an overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprises a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal, and preferably generally square, array of individual test structures.

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It should be emphasised that a mark in accordance with the invention is an overlay metrology mark, in which a mark portion is directly associated with each of the first and second layer to provide a directly measurable indication of the misregistration or overlay error between the layers under investigation.

25 In particular, each mark portion is preferably developed in or on the surface of the wafer layer in such direct association. For example, each mark portion may be printed onto the wafer layer, for example using the same technique which is used to apply the circuit pattern, and for example using photolithographic methods. Alternatively, a mark may be a latent image. The two mark portions,

comprising the complete overlay metrology mark, are imaged together to obtain a quantification of any overlay error.

5 The invention discloses novel target designs that address the disadvantages of the existing technology, in particular offering significantly improved accuracy, without sacrificing advantages in relation to speed of processing and otherwise.

10 The invention exploits the realisation that effective information about alignment in two directions may be given by a single square array exploiting entirely conventional imaging techniques, such as the bright field techniques commonplace in the prior art. Scanning this pattern in two dimensions, more specifically orthogonal X-Y scanning parallel to the two linear directions of the array, yields information about misalignment in both directions. This  
15 offers the potential to yield an overlay error measurement representative of layer misalignment in two dimensions from a single marked region using standard or specifically developed image analysis techniques to determine the misregistration between the two patterns. More complex patterns involving two or more regions in each mark, each adapted to measure misalignment in a  
20 particular direction, are not necessary, provided a single accurately disposed array of individual test structures in accordance with the invention is laid down upon each layer, or associated with each pattern, as the case may be.

A further advantage is that existing metrology tools may be simply adapted to  
25 their measurement, avoiding the costs involved in retooling that radically different methods would require.

Each mark portion is associated with a layer under test, so that the measured overlay error is representative of the misalignment between the respective  
30 layers. Overlay metrology marks in accordance with the invention are suited to

measurement of overlay errors between layers, in particular but not limited to consecutive layers. Where the overlay mark is used to aid measurement of misregistration between different layers, the first mark portion is laid down upon a first lower layer, and the second mark portion is laid down upon a second layer above the said first layer, in particular on an uppermost layer, such that the test structures of the lower layer are detectable through the upper layer. The upper mark portion serves as an alignment marking, and the lower mark portion as the reference marking.

- 10 The test structures comprising each mark portion are disposed in each case as a single two dimensional array with an orthogonal arrangement. This should be understood to mean that each array comprises an arrangement of individual test structures forming a plurality of parallel rows and columns, the row and column directions being at right angles to each other. In use these should
- 15 correspond to the mirror angles of the optical equipment used for image analysis. The structures form a repeating array. For most applications a substantially square array, with generally constant spacing between test structures throughout the array, will be preferred. In certain cases, a functionally varying spacing between adjacent rows and/or columns
- 20 respectively in a column/ row direction as the case may be useful for particular functionality, provided always that the orthogonal relationship of rows and columns is maintained.

Preferably the spacing between test structures in the array comprising the first

25 mark portion and the spacing between test structures in the array comprising the second mark portion is equivalent. In particular both are square arrays of generally equal spacing.

The overall mark portion preferably also has a generally square outline. It is

30 desirable if asymmetries are to be avoided. However minor deviations in

- particular are unlikely to be significant. Moreover, the requirement for an orthogonal array of successive rows and columns does not preclude designs where individual test structures are absent from a limited portion of the sites defined thereby. Such gaps might be incorporated for example to add readable  
5 information, or to include further mark features giving such give additional information. Such gaps/ additional marks are preferably located so as to maintain symmetry of the structure in the mark portion and/ or about the intended optic axis of the imaging apparatus.
- 10 The dimensions of each test structure within each array and the spacing thereof will be optimally determined by and are therefore preferably set with reference to the resolution limit of the imaging microscope. Typically therefore each test structure will have a width of around 0.5 to 2  $\mu\text{m}$ . Spacing  
15 between test structures in the array will preferably be between one and four structure widths. This will maximise feature density at the resolution limit of the imaging device. Any specific design embodying the principles of the invention will increase the number of feature transitions when compared with many previous designs. Each array may comprise several test structures in each direction, preferably at least five, while fitting comfortably into a  
20 conventional mark area. The additional image detail provides more information content in the image, providing for an improvement in measurement precision.

The individual test structures making up each array are preferably  
25 substantially identically sized and shaped. Each test structure conveniently has generally square geometry.

Individual test structures may optionally be made using design rule sized sub-structures to address issues of process induced inaccuracy, as is well known.

Suitable arrangements, familiar to those skilled in the art, include parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns. Sub-structure dimensions are set by design rule limits, being typically for present techniques of the order of 100 to several hundreds of nanometres. However advances in manufacturing processes are likely to further reduce these dimensions in the future.

In use with a standard imaging device, the orthogonal arrays making up each mark portion are to be aligned with the vertical and horizontal grid directions of each array (ie the rows and columns formed by the test structures) parallel to each other and to the X-Y symmetry lines of the imaging device. It has been noted that optimal performance depends on measurement being centred on the optic axis of the imaging device. Two embodiments are proposed to facilitate this.

In a first embodiment the arrays of test structures making up the first and second mark portions are disposed such that the first portion overlays the second portion and that the test structures at least to some extent are intercalated, especially in both directions. That is, the test structures of the second portion are arrayed within the gaps between the test structures of the first portion and visible therebetween. In particular, each test structure in the second portion is located at a point sitting at or in close proximity to the diagonal centre of a notional square bounded at each corner by test structures of the first portion.

The mark in accordance with the invention is an overlay metrology mark, and it follows that the two mark portions are imaged together to measure the overlay error between the two layers under test, with the intercalated structures

of the lower layer visible in the gaps between the structures of the upper layer. The geometry of this embodiment thus lends itself particularly to an overlay metrology, and the patent gives a particularly effective method of measuring overlay error in two dimensions.

5

Preferably, the two test portions are laid down with generally co-located centres, the common centre intended to correspond to the optic axis of the imaging system in use, but it will be understood that minor asymmetry in this regard, especially at the edges of the structure will not seriously degrade measurement accuracy as long as the interlaced arrangements is maintained.

10

In this embodiment, the design is optimised if test structures in each array are spaced with a pitch of around three to four times the width of an individual test structure. This provides adequate gaps in the array comprising the upper mark portion for visibility of test structures in the lower mark portion therethrough.

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In a second embodiment the test structures making up the first and second mark portions are disposed such that the first portion is laterally spaced from the second portion in a spacing direction parallel to a horizontal or vertical direction of the square arrays such that a notional line in the spacing direction can be drawn about which each array exhibits mirror symmetry. In use this will correspond to one of the mirror axes of the imaging device, with the centre point of this notional line equidistant from each mark portion intended to correspond to the optic axis of the imaging system. Each mark portion will preferably comprise an identical pattern of test structure.

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In this second embodiment arrays, and preferably square arrays, making up the first and second mark portions are laid down so as to be generally adjacent with the centroid of the combined mark preferably generally at the optic axis

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of the imaging device. Again, this effectively exploits the overlay metrology technique to measure overlay error between the two layers with which the mark portions are associated, and in particular allows measurement in two dimensions even if only a single mark portion is provided in association with  
5 each layer.

In this embodiment, the design is optimised if test structures in each array are spaced with a repeat distance, and in particular a constant periodicity, of two to three structure widths, in particular around two, i.e. so that the spacing  
10 between test structures is the same as the width of an individual structure.

In both of the foregoing principal embodiments, the overlay metrology mark comprised of the first and second mark portions is preferably so located in use that the centroid of the overall mark corresponds generally to the optic axis of  
15 the imaging apparatus. Other patterns which also conform to this general principal are also likely to be preferred as embodiments of the present invention.

The test structures making up the array comprising each mark portion may be  
20 laid down by any suitable technique known to those skilled in the art, in particular the photolithographic techniques above described.

In a preferred embodiment a recognition key is provided for use in association with an overlay mark as hereinbefore described. In accordance with the  
25 embodiment an identification portion is provided in association with a first mark portion, comprising a simple optically readable mark divided into a small number of pattern areas in each of which areas a marking may be present or absent, the pattern of such markings providing a unique identification key so as to serve to identify the first mark portion.

An identification portion in accordance with the invention is associated with the alignment mark and gives a simple digital identification of the alignment mark, ensuring the correct mark is selected. The identification portion thus acts as a pattern recognition key.

5

A similar identification portion may be associated with other marks on a wafer, whereby the embodiment of the invention comprises an overlay metrology mark system for the whole wafer ensuring the correct marks are selected at all times. The probability of locating the wrong overlay metrology mark can be reduced by varying the pattern in adjacent marks, increasing the distance to a potentially confusing pattern recognition key.

10

In particular, the identification portion is laid down with the first mark portion, for example at the same time and for example on the same layer. The identification portion is conveniently located proximal to the first mark portion, for example comprising a part thereof.

15

The recognition key comprises a simple pattern exhibiting a small number of discrete alternative shapes to give a digital identifier. The pattern is adapted to be optically readable by standard imaging equipment at the same time as the primary alignment mark is imaged, requiring no major equipment modification and only minimal modification to image analysis. The recognition key is preferably laid down by the same process as the primary mark, for example employing photolithographic techniques. However, the pattern making up the recognition key is designed to be optically imaged for recognition purposes only, and not for determination of alignment differences. The structure can accordingly be made from structural element(s) which optimise this aspect, and might therefore be substantially larger than the structures making up the primary alignment mark.

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The recognition key pattern comprises a small number of pattern areas, for example between four and eight, in each of which areas a marking may be present or absent, the pattern of such markings thus providing the unique identification. In particular, in each pattern area a marking is either  
5 substantially entirely present or substantially entirely absent. The arrangement of which pattern areas are present and which are absent gives the unique key. For example, for simplicity it might be preferable if a mark is absent in a single pattern area.

10 Preferably, the recognition key pattern has a generally square or rectangular outline. This is particularly the case where the corresponding primary mark has generally square or rectangular symmetry. In particular, the horizontal and vertical directions of such a square or rectangular outline correspond to the horizontal and vertical directions of a similarly square or rectangular  
15 overlay mark, and in use with the x and y directions of symmetry in the optical imaging apparatus. As a consequence of this geometry, each pattern area is similarly preferably square or rectangular. The recognition key pattern then preferably comprises a linear or two-dimensional array of such pattern areas, for example consisting of between one and four such areas in each of a row  
20 and column direction, corresponding in use to the x and y directions in the optical imaging apparatus.

Each pattern area preferably has dimensions of between 1 and 4  $\mu\text{m}$ , and particularly preferably comprises a 1  $\mu\text{m}$  square. All pattern areas making up  
25 the recognition key pattern are preferably identically sized and shaped.

In particular, the key pattern comprises a square or rectangular area subdivided into a two dimensional array of square or rectangular pattern areas. This gives a highly readable identification mark, maintaining the square or

rectangular symmetry of many of the alignment marks with which it is intended to be used, and accordingly easily readable by the imaging equipment. Suitable overall pattern dimensions are from 2 to 8  $\mu\text{m}$ , allowing pattern area dimensions of 1 to 2  $\mu\text{m}$  for ease of imaging. In particular pattern areas are 1 to 2  $\mu\text{m}$  squares.

In a particular embodiment the recognition key pattern comprises a square divided into four equal sub-square pattern areas as above described. Each sub-square pattern area is either present or absent in the recognition key pattern. Mostly preferably, the recognition key pattern comprises a generally L-shaped mark, wherein there are four such sub-square pattern areas in one of which a mark absent. The mark provides four distinct patterns (dependent upon the orientation of the L-shape) which are easily readable and distinguished. This is sufficient for many purposes.

It is well known that optimal performance depends on measurement being centred on the optic axis of the imaging device. Overlay marks are usually symmetric about this centre, with the overlay error being the measured displacement of the centres. Conveniently, to avoid introducing asymmetry, the recognition key may be located at the centre. Alternatively, a plurality of recognition keys are provided away from the centre.

The advantages of existing target designs are retained. The measurements are made from a single image so that speed of measurement is not compromised. The measurement is made using an optical image, so that existing imaging tools can be used. Overlay error may be quantified using any suitable known or specifically developed image processing technique.

Thus, in accordance with the present invention in a second aspect a method for providing an overlay metrology mark to determine the relative position

between two or more layers of an integrated circuit structure comprises the steps of:

laying down a first mark portion in association with a first layer;

and laying down a second mark portion in association with a second layer;

- 5 wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures.

Similarly, in accordance with the present invention in a third aspect a method for determining the relative position between two or more layers of an  
10 integrated circuit structure comprises the steps of:

laying down a first mark portion in association with a first layer;

laying down a second mark portion in association with a second layer;

wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures;

- 15 optically imaging the two mark portions in a horizontal and vertical array direction;

collecting and digitizing the image;

numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

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It is important to emphasise that each mark portion making up the overlay metrology mark is laid down in direct association with the associated layer, and in particular is preferably developed within or on the surface of the said layer. For example each mark portion is printed on the said layer. Each mark  
25 portion is preferably laid down by a photolithographic process.

In a preferred embodiment of the method of the invention, the overlay metrology mark incorporates an identification mark serving as a recognition key as hereinbefore described. The method thus comprises, in association with

the step of laying down of an alignment mark portion associated with a second layer, and for example contemporaneously therewith, laying down in association with the said mark portion an identification portion comprising a simple optically readable mark divided into a small number of pattern areas in each of which areas a marking may be present or absent, the  
5 pattern of such markings providing a unique identification key so as to serve to identify the alignment mark portion.

Optical imaging of the mark is preferably carried out using imaging  
10 microscopy, and for example bright field microscopy. Other preferred features of the methods will be understood by analogy with the foregoing.

The invention will now be described by way of example only with reference to figures 1 to 2 of the accompanying drawings, in which:

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Figures 1a to 1c are general schematics of a mark in accordance with a first principal embodiment of the invention comprising superimposed mark portions;

20 Figure 2 is a general schematic of a mark in accordance with a second principal embodiment of the invention comprising adjacent mark portions;

Figure 3 is a plan view of a suitable identification recognition key for use in accordance with a preferred embodiment of the invention;

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Figure 4 illustrates use of the key of figure 3 in association with the marks of figure 1;

Figure 5 illustrates example substructures for a mark structure for use with a  
30 mark in accordance with the invention.

The overlay metrology mark comprises a first or reference mark portion on a first lower layer and a second or alignment mark portion on a second layer above the first layer, for example an uppermost layer. Where complete marks  
5 are illustrated in the figures, the second mark portion is represented by darker grey-shaded structures. The first mark portion, configured to be at least partially visible in conjunction with the second, is represented by lighter grey-shaded structures.

10 In each case the invention lies in the arrangement of test structures in a repeating array. The structures and any sub-structures making up the test structures are formed using any suitable processes. Typically these will include lithographic processes that are generally known in the art. Misalignment is measured using imaging systems and image analysis  
15 techniques, which may be standard systems and techniques that are generally known in the art or systems and techniques modified to be optimized specific to the marks in accordance with the invention.

Figure 1 illustrates a top plan view of three alternative overlay metrology  
20 marks according to one embodiment of the invention. In each case the mark is shown in the intended configuration that results when the tested layers of a structure are in proper alignment. The mark consists of two mark portions, one on each layer, comprising substantially identical square arrays of test structures overlaid into an interlocking pattern, whereby the test structures of  
25 the second mark portion lie at the centres of notional squares bounded at the corners by test structures in the first mark portion. Each array also has an overall square shape.

Figure 1a illustrates the simplest example. Identical square arrays are laid down relatively shifted by half a repeat in both directions to make up the overall structure. This design lacks central symmetry.

- 5 Figure 1b illustrates an arrangement to address this and allow the two arrays to be laid down with a common centroid. The first mark portion is larger by one pattern repeat in both directions, and offset relative to the second by half a pattern repeat in both directions, to maintain rotational symmetry about the common centroids. This common centroid should correspond to the optic axis  
10 of the imaging system in use, with mirror axes of the imaging system parallel to the rows and columns of the squares. Given appropriate axis orientation of a suitable imaging device the rows in each array may serve for x-axis registration measurements and the columns for y-axis registration measurements. The simple mark, with a single array comprising the mark  
15 portion on a layer, can thus give two dimensional registration information.

Each of the mark portions consists of a square array of repeating test structures. In the examples the period of repeat is constant. Each of the test structures in the example is also square in general outline. Each is shown solid  
20 in this plan view, but it will be well understood that it could comprise multiple sub-structures at a design rule level (examples of which are given below) for reasons that will be familiar. In a specific implementation of the example mark each test structure comprises a 1  $\mu\text{m}$  square. Lateral spacing between squares is then around 3  $\mu\text{m}$  to provide the necessary gaps for the interlocking  
25 arrangement of the two arrays. Dimensions are set to maximise feature density within a normal mark area and hence accuracy, subject to the resolution limit of a typical imaging system. The measurements will vary in practice, depending on the required accuracy and the resolution limit of the imaging system.

Figure 1c illustrates an alternative arrangement. Whereas in Figure 1b the arrays are continuous across the centre, in this arrangement a gap is provided in the centre of the array, into which an identification key mark could be included with the overlay layer to ensure that correct reference and overlay are matched. This is optional, and may limit the effectiveness of the target design due to loss of data.

Figure 2 illustrates a top plan view of an overlay metrology mark according to a second embodiment of the invention. The mark is shown in the intended configuration that results when the tested layers of a structure are in proper alignment. The mark consists of two mark portions, one on each layer, comprising substantially identical square arrays of test structures. Each array also has an overall square shape.

The two arrays are laid down displaced apart about a notional line which can be drawn parallel to the array rows so as to form a notional mirror symmetry line for each square. The centre of this notional line should correspond to the optic axis of the imaging system in use, with mirror axes of the imaging system parallel to the rows and columns of the squares. As before, with appropriate axis orientation of a suitable imaging device the rows in each array may serve for x-axis registration measurements and the columns for y-axis registration measurements so that the simple mark, with a single array comprising the mark portion on a layer, can give two dimensional registration information.

Each mark portion is preferably laid down by a photolithographic process. As before, each of the test structures in the example is also square in general outline and shown solid but could comprise multiple sub-structures at a design rule level. In a specific implementation of the example mark each test

structure comprises a 1  $\mu\text{m}$  square. Lateral spacing between squares is also around 1  $\mu\text{m}$ . Dimensions are again set to maximise feature density subject to the resolution limit of a typical imaging system.

5 Figure 3a shows a basic recognition key suitable for use with the overlay metrology mark of the invention in accordance with a preferred embodiment thereof. The mark is shown in top plan view. Increasingly, new measurement structures do not provide an easy pattern recognition target as there is no isolated well-resolved image in the resist. The key comprises a specific mark  
10 printed in the resist layer. The mark consists of a 2  $\mu\text{m}$  square mark area subdivided into a two by two array of 1  $\mu\text{m}$  square pattern areas. Three of these are covered by the mark material and one absent. The effect is to produce a key comprising a 2  $\mu\text{m}$  square from which one corner is omitted, giving a general L-shape.

15

Any corner may be omitted, allowing four unique pattern recognition targets to be created as illustrated in figure 3b. The simplicity of the design makes this easy to image, and easy to distinguish between the four targets, so that the key provides a clear digital identifier of a given overlay mark with which it is  
20 associated, and greatly assists in ensuring the correct overlay mark is imaged. Overlay targets can be positioned nearby but will be safe from pattern recognition error if the keys are different. The probability of locating the wrong target can be reduced by varying the omitted corner in adjacent targets, increasing the distance to a potentially confusing pattern recognition key.

25

Figure 4 illustrates use of the key of figure 3 in association with the marks of figure 1. In Figure 4a a key is placed adjacent a mark of the type shown in Figure 1b. In Figure 4b a key is placed centrally within a mark of the type



shown in Figure 1c. These examples are illustrative only of the various arrangements that could be envisaged.

Figure 5 illustrates example substructures for a mark structure for use with a  
5 mark in accordance with the invention. A single individual test structure from  
those making up each array of a mark in accordance with the invention is  
shown above, being a 1  $\mu\text{m}$  square. Such an individual test structure may  
optionally be made using design rule sized sub-structures to address issues of  
process induced inaccuracy, as is well known. In the illustrated four examples  
10 below, the 1  $\mu\text{m}$  square comprises patterns of square or rectangular  
substructures to form the required shape. Because the small features are not  
resolved, they are not individually visible through the microscope, giving the  
appearance of a single contiguous structure. The mark-space ratio of the sub-  
resolution features can be adjusted to meet the optimal performance criteria of  
15 the printing process.

CLAIMS

1. An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal array of individual test structures.
2. An overlay metrology mark in accordance with claim 1 wherein each mark portion is developed within or on the said layer.
3. An overlay metrology mark in accordance with claim 2 wherein each mark portion is printed on the said layer by a microlithographic process.
4. An overlay metrology mark in accordance with any preceding claim wherein each mark portion comprises a single two dimensional generally substantially square array of individual test structures with generally constant spacing between test structures throughout the array.
5. An overlay metrology mark in accordance with any preceding claim wherein the spacing between test structures in the array comprising the first mark portion and the spacing between test structures in the array comprising the second mark portion is equivalent.
6. An overlay metrology mark in accordance with any preceding claim wherein each mark portion has a generally square overall outline.
7. An overlay metrology mark in accordance with any preceding claim wherein each test structure has a width of around 0.5 to 2  $\mu\text{m}$ .

8. An overlay metrology mark in accordance with any preceding claim wherein spacing between test structures in the array is between one and four structure widths.
- 5
9. An overlay metrology mark in accordance with any preceding claim wherein the individual test structures making up each array are substantially identically sized and shaped and have generally square geometry.
- 10
10. An overlay metrology mark in accordance with any preceding claim wherein the individual test structures comprise arrangements of design rule sized sub-structures.
- 15
11. An overlay metrology mark in accordance with claim 10 wherein the arrangements of design rule sized sub-structures are selected from parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any
- 20
- combinations of these or other like patterns.
12. An overlay metrology mark in accordance with claim 10 or 11 wherein sub-structures are of design rule dimensions.
- 25
13. An overlay metrology mark in accordance with any preceding claim wherein the arrays of test structures making up the first and second mark portions are disposed such that the first portion overlays the second portion and that the test structures of second portion are arrayed within the gaps between the test structures of the first portion and visible
- 30
- therebetween.

14. An overlay metrology mark in accordance with claim 13 wherein each test structure in the second portion is located at the diagonal centre of a square bounded at each corner by test structures of the first portion.
- 5
15. An overlay metrology mark in accordance with any one of claims 1 to 12 wherein the test structures making up the first and second mark portions are disposed such that the first portion is laterally spaced from the second portion in a spacing direction parallel to a horizontal or vertical direction of the square arrays such that a notional line in the spacing direction can be drawn about which each array exhibits mirror symmetry.
- 10
16. An overlay metrology mark in accordance with claim 15 wherein each mark portion comprises an identical pattern of test structures.
- 15
17. A method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of:
- laying down a first mark portion in association with a first layer;
- 20 and laying down a second mark portion in association with a second layer;
- wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures.
- 25
18. A method for determining the relative position between two or more layers of an integrated circuit structure comprises the steps of:
- laying down a first mark portion in association with a first layer;
- laying down a second mark portion in association with a second layer;
- wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures;
- 30

optically imaging the two mark portions;  
collecting and digitizing the image;  
numerically analysing the digitized data to obtain a quantified  
measurement of the misalignment of the first and second mark portions.

5

19. The method of claim 18 wherein optical imaging of the mark is carried  
out using bright field microscopy.

20. The method of one of claims 17 to 19 wherein each mark portion is  
developed within or on the said layer.

10

21. The method of one of claims 17 to 20 wherein each mark portion is laid  
down by a microlithographic process.

22. A mark or method substantially as hereinbefore described with reference  
to the accompanying drawings.

15

1/3

Figure 1a

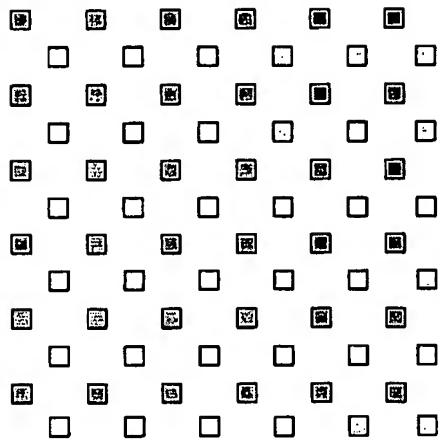


Figure 1b

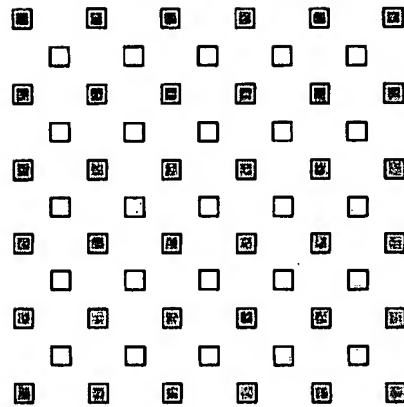


Figure 1c

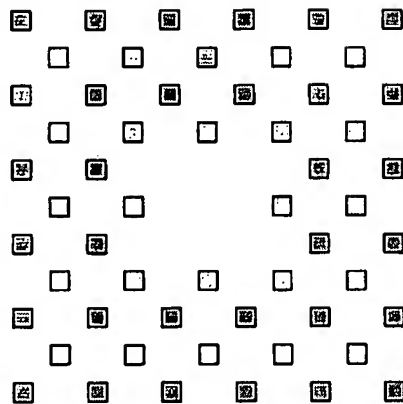


Figure 2

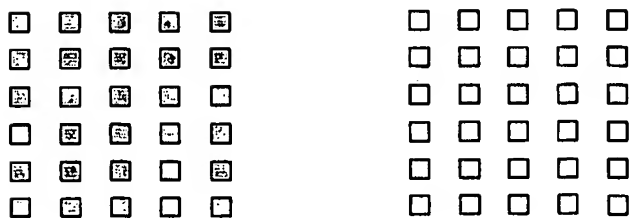


Figure 3a

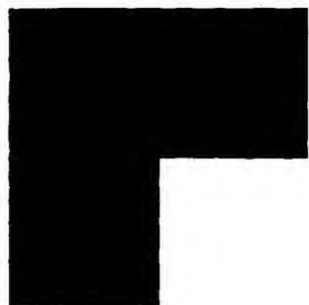


Figure 3b



Figure 4a

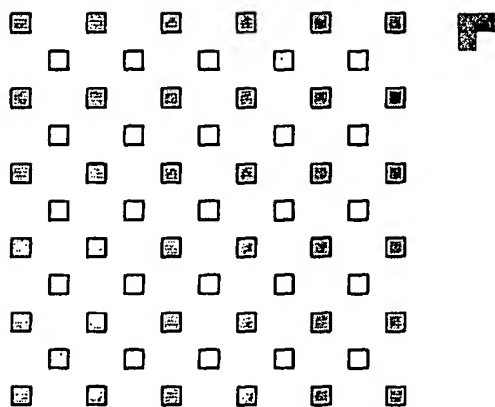
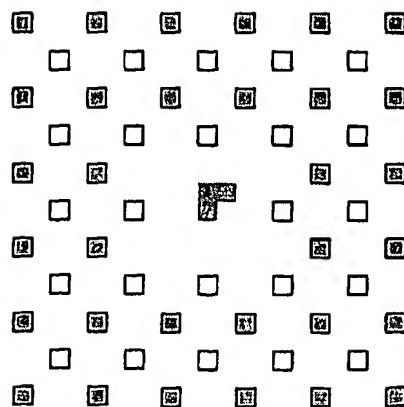
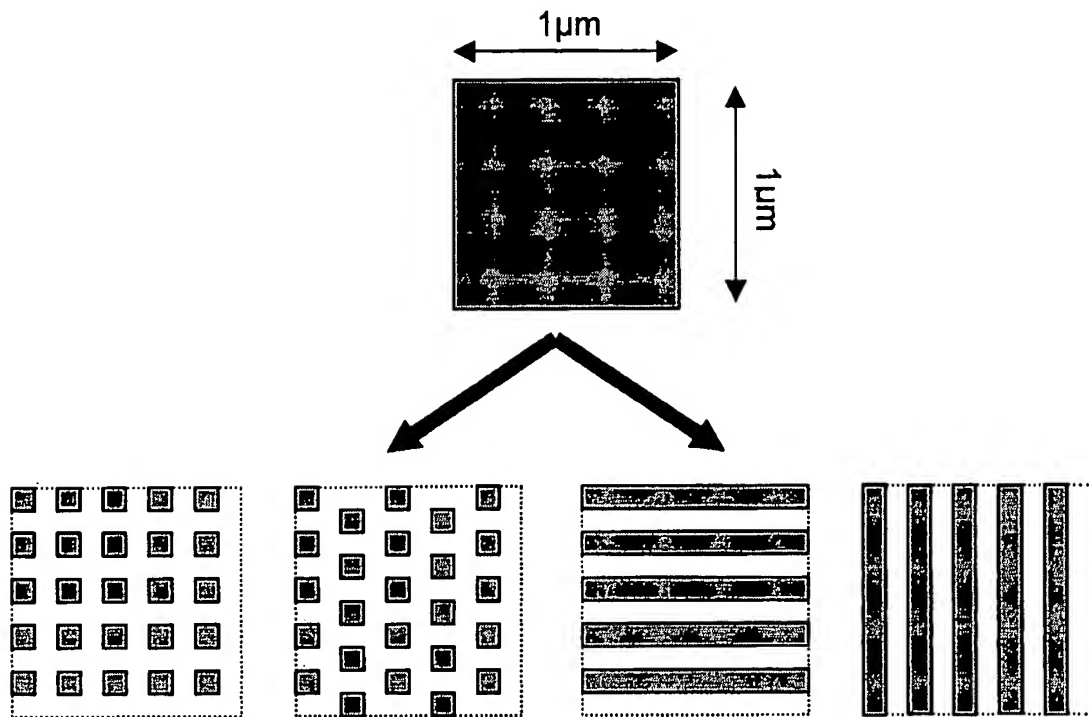


Figure 4b



3/3

Figure 5





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(54) Title: **OVERLAY METROLOGY MARK**

(57) Abstract: An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with and in particular developed on a first layer and a second mark portion associated with and in particular developed on a second layer, wherein the first and second mark portions together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone such that the mark structures in each test zone are in alignment in a first direction within the test zone but are substantially at 90° with respect to the mark structures of at least one other test zone in alignment in a second direction, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions. A method of marking and a method of determining overlay error are also described.



**WO 2004/090979 A2**

### Overlay Metrology Mark

The invention relates to overlay metrology during semiconductor device  
5 fabrication, and in particular to an overlay alignment mark to facilitate  
alignment and/or measure the alignment error of two layers on an integrated  
circuit structure during its fabrication.

Modern semiconductor devices, such as integrated circuits, are typically  
10 fabricated from wafers of semiconductor material. In particular, a wafer is  
fabricated comprising a succession of patterned layers of semiconductor  
material.

Circuit patterns are fabricated using a variety of long established techniques,  
15 for example making use of lithographic techniques. Precise positioning and  
alignment during fabrication is of great significance in the manufacture of  
accurate patterns. For example, alignment control of the exposure tool is  
important in ensuring a consistent process. Alignment methodologies are  
established in this regard, in which statistical and modelling techniques are  
20 used to determine the alignment of a reticle with a pattern created by or in  
association with the exposure tool to facilitate alignment of the exposure tool.  
The technique typically exploits images generated within the exposure tool  
optics, or projected onto the wafer by the exposure tool optics. Similar model-  
based and statistical methods have been employed to align for example an  
25 exposure tool during pattern fabrication.

Although such alignment technology has an established utility, and is  
important in device fabrication, it relates to alignment of fabrication tooling  
only. This can be a limitation in relation to integrated circuit structures  
30 comprised of a succession of pattern layers of semiconductor material where it

is desirable in relation to such wafers to provide a methodology enabling a determination of the misregistration between fabricated layers themselves.

Overlay metrology in semiconductor device fabrication is used to determine how well one printed layer is overlaid on a previously printed layer. Close alignment of each layer at all points within the device is crucial for reaching the design goals and hence the required quality and performance of the manufactured device. It is consequently of importance for the efficiency of the manufacturing process that any alignment error between two patterned layers on a wafer, especially successive patterned layers can be measured quickly and accurately. It is similarly important to be able to measure any alignment error between successive exposures in the same layer, and where reference is made herein for convenience to two layers it will be understood where appropriate to apply equally to two exposures in the same layer.

15

Misregistration between layers is referred to as overlay error. Overlay metrology tools are used to measure the overlay error. This information may be fed into a closed loop system to correct the overlay error.

Current overlay metrology employs optically readable target patterns, printed onto the successive layers of a semiconductor wafer during fabrication. The relative displacement of two successive layers is measured by imaging the patterns at high magnification, digitizing the images, and processing the image data using various known image analysis algorithms to quantify the overlay error. Overlay metrology techniques thus involve the direct measurement of misregistration between patterns provided in direct association with each of the fabricated layers under investigation. In particular, patterns are developed in or on the surface of each of the layers, or may be latent images, rather than images generated within or projected from the optics of an imaging instrument.

The pattern of the target mark may be applied to the wafer by any suitable method. In particular, it is often preferred that the mark is printed onto the wafer layers for example using photolithographic methods. Typically, the same technique is used to apply overlay target marks on each of two wafer layers to be tested to enable alignment information to be measured which is representative of the alignment of the layers. Accuracy of layer alignment should correspond to accuracy of circuit pattern alignment within the fabricated wafer.

10

Current overlay metrology is normally practised by printing targets with rectangular symmetry. For each measurement two targets are printed, one in the current layer and one in a previous layer, or one in association with each pattern in a common layer. The choice of which previous layer to use is determined by process tolerances. The two targets have a nominally common centre, but are printed with different sizes so that they can be differentiated. Normally, but not always, the target printed in the current layer is the smaller of the two targets. An overlay measurement in such a system is the actual measured displacement of the centres of the two targets.

20

Current preferred practice is that the size of the targets is designed such that both can be imaged simultaneously by a bright-field microscope. Imaging considerations determine that the larger of the two targets is typically a 25µm square on the outside. This arrangement permits capture of all of the necessary data for the performance of the measurement from a single image. Measurements at a rate of one in every two seconds or less are possible using current technology.

The procedure necessarily requires that the target and its image are symmetric, since otherwise there is no uniquely defined centre point. Without symmetry

30

there is an uncertainty in the measurement, which may be more than can be tolerated. Within that general requirement, optimal sizes and shapes of current designs of targets to be measured are well known. The targets are positioned in the scribe area at the edge of the fabricated circuit.

5

It is generally desirable that the measurement targets maintain axial symmetry about the optical axis of the measurement tool, since accurate measurement requires very close control of image aberrations. To achieve this it can also therefore be advantageous to use marks at or with symmetry centred about the system axis.

10

Marks exhibiting symmetry are usually aligned in a known and consistent relationship relative to the crystal lattice of the wafer. Where this defines "X" and "Y" directions these are conveniently used as reference directions for the imaging apparatus. The "X" and "Y" planes are more specifically relevant to the wafer than they are to the optics, but it is normal to choose to align the wafer such that "X" corresponds to the horizontal and "Y" to the vertical as viewed through the microscope. It is possible in principle to measure at any other orientation, but for many mark symmetries advantages are conferred if the marks are arranged to have symmetry about what are conventionally termed the "X" and the "Y" axes, which allows the optimum performance to be obtained from the metrology apparatus.

15

20

In most prior art systems, measurements are therefore made from the targets by computing a centre line for each different target. The overlay measurement is the difference in the centre lines. Most of the target designs in general use permit measurement of the vertical and horizontal overlay displacement from a single image.

25

Measurement errors must be controlled to a very small amount. Errors known to arise are classified as random errors, characterized by determination of measurement precision; and systematic errors, characterized by tool induced errors, tool-to-tool measurement differences and errors introduced by asymmetry in the targets being measured. Successful application of overlay metrology to semiconductor process control is generally held to require that, combined, these errors are less than 10% of the process control budget. This measurement error budget is in practice in the range 1 to 5 nm, and will remain so in the foreseeable future.

Measurement precision is easily determined by analysis of the variations of repeated measurements. Different forms of precision may be determined by well known appropriate methods, allowing determination of the static, short-term and long-term components of precision.

Determining the contribution of the measurement tool alone to errors is achieved by comparing measurements made with the target in its normal presentation with a measurement made after rotating the target by 180° with respect to the imaging system. Ideally the measurement will simply change sign. The average of the measurements at 0° and 180° is called *Tool Induced Shift* (TIS), as is well known to those skilled in the art, and is widely accepted as a measure of the tool's systematic error contribution. Measurements of TIS differ from tool to tool and with process layer. Subtraction of the estimated TIS error from the measurements allows removal of the TIS error from the measurements, but at the expense of the additional time taken to measure the target twice.

Different tools, even when of the same type, will make slightly different measurements, even after allowing for precision and TIS errors. The

magnitude of this error can be determined experimentally by comparing the averages of repeated measurements at  $0^\circ$  and  $180^\circ$  on two or more tools.

The contributions of precision, TIS and tool-to-tool differences are normally  
5 combined through a root-sum-square product, or alternative appropriate  
method, to determine the total measurement uncertainty due to the  
measurement process. The total measurement uncertainty must be less than  
10% of the overall overlay budget for the process if the metrology is to have  
value. Existing measurement tools and procedures achieve a total uncertainty  
10 within that required for current process technologies but insufficient for future  
requirements.

By contrast, although the contribution of asymmetry in the measurement target  
itself is widely understood it is not normally determined. It is known that in  
15 many cases it can be much larger than the tool contribution to measurement  
uncertainty. There are two sources of error to be considered:

1. Imperfection in the manufacture of the target which leads to an  
uncertainty in its location. An example of this is physical asymmetry  
of the target, caused perhaps by uneven deposition of a metal film.
- 20 2. Difference in the displacement of the two layers at the measurement  
target and the genuine overlay of the same layers in the device being  
manufactured. These can arise from errors in the design and  
manufacture of the reticles used to create the patterns on the wafer,  
proximity effects in the printing process and distortion of the films after  
25 printing by other process steps.

These measurement errors represent a practical limitation of the current state  
of the art which causes severe problems in the application of overlay  
metrology to semiconductor process control.

Improvements to the first of these problems can sometimes be achieved by fabricating the features in the measured targets from much smaller objects - lines or holes. The common term for this technique is "segmentation". These smaller features are printed at the design rule for the process, currently in the  
5 range 0.1-0.2  $\mu\text{m}$ , and are grouped close together. They are too small to be individually resolved by the optical microscopes used in overlay metrology tools. The small features are grouped into larger shapes in the pattern of traditional overlay targets. The use of small features avoids some of the mechanisms causing imperfections in the shape of the manufactured targets, in  
10 part by taking advantage of the optimization of the manufacturing process for objects of this size and shape.

A further problem is introduced by the size of the targets, which are a significant fraction of the space available in the scribe area surrounding the  
15 devices being fabricated. It is desired that the size of these areas be reduced, which means that it is also highly desirable that the measurement targets be made smaller. However, the size of the target cannot be reduced too much, since accurate measurement requires that the measured features are not smaller than the resolution of the microscope system, and achieving good precision  
20 requires that as many as possible of such features are visible in the image.

It has been shown (Smith, Nigel P.; Goelzer, Gary R.; Hanna, Michael; Troccolo, Patrick M., "*Minimizing overlay measurement errors*", August 1993, Proceedings of SPIE Volume: 1926 Integrated Circuit Metrology, Inspection, and Process Control VII, Editor(s): Postek, Michael T) that space  
25 must be left between the features printed from the two layers else the proximity of one to another causes an error in the measurement. The magnitude of this error depends on the resolution of the imaging microscope system, but must be 5  $\mu\text{m}$  or greater in practical designs if the measurement



error is to be contained within practical limits. This proximity effect further limits the extent to which the size of the targets can be reduced.

However, high speed is one of the key advantages of existing overlay metrology practice, and any process development must not lose this advantage if it is to be viable in production use. This requirement means that uncertainty reduction by the use of repeated measurements is highly undesirable. There is thus a general desire to develop alternative overlay patterns and/or analysis methods which apply the basic principles of existing metrologies but in a manner that mitigates some or all of these errors to produce an improved fabrication metrology, and in particular a metrology offering improved accuracy without substantial loss of throughput speed. Moreover, it is desirable to use existing imaging tooling, and so desirable to retain the generally square or rectangular mark geometry familiar in the art.

15

In accordance with the present invention in a first aspect an overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprises a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein the first and second mark portions together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone such that the mark structures in each test zone are in alignment in a first direction within the test zone but are substantially at 90° with respect to the mark structures of at least one other test zone in alignment in a second direction, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions.

30

It should be emphasised that a mark in accordance with the invention is an overlay metrology mark, in which a mark portion is directly associated with each of the first and second layer to provide a directly measurable indication of the misregistration or overlay error between the layers under investigation.

5 In particular, each mark portion is preferably developed in or on the surface of the wafer layer in such direct association. For example, each mark portion may be printed onto the wafer layer, for example using the same technique which is used to apply the circuit pattern, and for example using photolithographic methods. Alternatively, a mark may be a latent image. The two mark portions,

10 comprising the complete overlay metrology mark, are imaged together to obtain a quantification of any overlay error.

The invention discloses novel target designs that address the disadvantages of the existing technology, in particular offering generally improved

15 measurement performance in relation to the control of errors discussed above without sacrificing advantages in relation to speed of processing and otherwise.

In order to give effective X-Y information, many prior art mark designs which

20 are similarly made up of rectangular test structures divide the mark area into four zones, respectively corresponding to the X and Y directions for each of the reference and overlay markings. Given the symmetry of the optics commonly used, there can be advantages if these are disposed around the optic axis of the instrument, in a square array.

25

The present invention exploits the realisation that by combining the test sections in this novel way, test zones can be laterally spaced about the optic axis of the imaging equipment, rather than rotationally disposed therearound, so that each test zone can lie on a mirror axis of the imaging equipment in use

30 and reduce this problem.

The key to achieving this objective lies in the novel way in which the mark within a test zone is constituted. In a test zone in accordance with the invention a first mark section from a first layer and a second mark section  
5 from a second layer co-operate together and are adjacently disposed such that each test zone comprises co-operably disposed and aligned mark structures from both layers under test. Combining mark structures from both layers in a single test zone in this way allows the overall pattern of multiple test zones to be simplified relative to typical examples in the prior art, and in particular then  
10 allows test zones to be laterally spaced about the optic axis without loss of X-Y information. The novel composition of each test zone is particularly suited to the specific features of overlay metrology technology, and exploits these to the full to provide an effective means of reducing asymmetry errors.

15 The preferred square or rectangular symmetry of the test zones can be retained. Accordingly, each test zone preferably has a generally square or rectangular outline shape, the rectangular directions corresponding to the said first and second directions and to the mirror axes of the imaging equipment in use. Generally square test zones are especially to be preferred. The lateral  
20 spacing means each pair of zones can be disposed in use to have mirror symmetry about an axis of the imaging apparatus, with the mid point at the optical centre thereof. Preferably, the test zones in a pair are identically sized and shaped. Where more than one pair is present all of the test zones may be identically sized and shaped, or different pairs may be differently sized and  
25 shaped. Where more than one zone pair is present, the mid points for each pair are co-located.

A particular advantage of the invention is that existing metrology tools may be simply adapted to measurement of the present target designs, avoiding the  
30 costs involved in retooling that radically different methods would require.

Each mark portion is associated with a layer under test, so that the measured overlay error is representative of the misalignment between the respective layers. Overlay metrology marks in accordance with the invention are suited to measurement of overlay errors between layers, in particular but not limited to consecutive layers. Where the overlay mark is used to aid measurement of misregistration between different layers, the first mark portion is laid down upon a first lower layer, and the second mark portion is laid down upon a second layer above the said first layer, in particular on an uppermost layer, such that the test structures of the lower layer are detectable through the upper layer. The upper mark portion serves as an alignment marking, and the lower mark portion as the reference marking.

In a simplest embodiment of the invention the number of test zones can be reduced to two. The first and second mark sections of the first zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the first (or overlay) mark portion and the second (or reference) mark portion. The first and second mark sections of the second zone are similar arrays but disposed at right angles thereto. Only two test zones are needed to give information in both X and Y directions.

These two test zones are laterally spaced along a line which is parallel to the direction of the test structures in one zone, and perpendicular in the other zone. As a result both test zones can be located generally on an axis of mirror symmetry of the scanning apparatus. Improved accuracy in overlay error measurements is offered by this closer association with the axis of symmetry of typical imaging apparatus.

In an alternative embodiment the mark comprises more than one pair of test zones. Each pair is laterally disposed equidistantly about a common centre in

one or other of the said two directions. In a particularly preferred embodiment, a single such pair is disposed in a first direction and a single such pair in a second direction. The first and second mark sections of each zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the first (or overlay) mark portion and the second (or reference) mark portion. The first and second mark sections of two zones are in the first direction and the first and second mark sections of the other two zones in similar arrays but disposed at right angles thereto. This may be achieved either in that a zone in each pair has mark structures oriented in each direction, or in that both zones in a pair have a common orientation perpendicular to that of the other pair.

These two test zones in each pair are laterally spaced in respectively an X and Y direction about common centres. In particular they are equidistantly spaced. As a result all test zones can lie about an axis of mirror symmetry of the scanning apparatus, which is not possible in conventional overlay marks comprising four test zones in a square array. The extra information such a four zone array offers can be retained without losing the preferred square or rectangular geometry.

20

The mark structures comprising each mark section are elongate rectangular structures in parallel array. It will be understood that provided the general elongate rectangular outline for these test structures is maintained, the structures need not be single monolithic rectangular structures. As will be familiar to those skilled in the art, each rectangular test structure may be made up of a series of sub structures. For example, each elongate rectangular test structure may comprise a row or column as the case may be of smaller constituent test structures, for example a row or column of squares.

Each elongate rectangular test structure and/or each constituent test structure may comprise sub structures down to design rule limits in the manner which will be familiar to address issues of process induced inaccuracy, as is well known. Suitable arrangements, familiar to those skilled in the art, include

5 parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any combinations or other like patterns. Sub-structure dimensions are set by design rule limits, being typically for present techniques of the order of 100 to several hundreds of nanometres.

10 However advances in manufacturing processes are likely to further reduce these dimensions in the future.

The mark sections each comprise elongate rectangular structures in a repeating array. Preferably the pitch is of constant period in each mark section.

15 Preferably the period is identical in all mark sections. In a particular preferred configuration, all rectangular test structures in a test zone, and more preferably in the whole mark, have identical widths and spacing. In this way, test structures from the overlay and test structures from the reference in a given test zone are all in alignment when the mark is correctly aligned. In particular,

20 each test structure abuts its neighbour to form in combination therewith a single elongate rectangular mark structure when in correct alignment.

Each test zone should preferably have a rectangular, and in particular a generally square outline. Given typical overall mark sizes of 25  $\mu\text{m}$ , each test

25 zone is conveniently around a 10 to 12  $\mu\text{m}$  square.

The dimensions of each test structure within each zone and the spacing thereof will be optimally determined by and are therefore preferably set with reference to the resolution limit of the imaging microscope. In one implementation

therefore each test structure will have a width of around 0.5 to 2  $\mu\text{m}$ . Spacing between test structures in the array will preferably be between one half and two structure widths, and in particular around 1 structure width. This will maximise feature density at the resolution limit of the imaging device. Any specific design embodying the principles of the invention will increase the number of feature transitions when compared with many previous designs. Each mark section then comprises several test structures in each direction, preferably at least five, while fitting comfortably into a conventional mark area. The additional image detail provides more information content in the image, providing for an improvement in measurement precision.

In use with a standard imaging device, the test structures making up each mark portion are to be aligned with the vertical and horizontal grid directions of each array parallel to the X-Y symmetry lines of the imaging device. It has been noted that optimal performance depends on measurement being centred on the optic axis of the imaging device. In use the optic axis of the imaging instruments will be located at a point generally equidistant between each test zone pair along a notional line between the centres thereof.

The test structures making up the array comprising each mark portion may be laid down by any suitable technique known to those skilled in the art, in particular the photolithographic techniques above described.

In a preferred embodiment a recognition key is provided for use in association with an overlay mark as hereinbefore described. In accordance with the embodiment an identification portion is provided in association with a first mark portion, comprising a simple optically readable mark divided into a small number of pattern areas in each of which areas a marking may be present or absent, the pattern of such markings providing a unique identification key so as to serve to identify the first mark portion.

An identification portion in accordance with the invention is associated with the alignment mark and gives a simple digital identification of the alignment mark, ensuring the correct mark is selected. The identification portion thus  
5 acts as a pattern recognition key.

A similar identification portion may be associated with other marks on a wafer, whereby the embodiment of the invention comprises an overlay metrology mark system for the whole wafer ensuring the correct marks are  
10 selected at all times. The probability of locating the wrong overlay metrology mark can be reduced by varying the pattern in adjacent marks, increasing the distance to a potentially confusing pattern recognition key.

In particular, the identification portion is laid down with the first mark portion,  
15 for example at the same time and for example on the same layer. The identification portion is conveniently located proximal to the first mark portion, for example comprising a part thereof.

The recognition key comprises a simple pattern exhibiting a small number of  
20 discrete alternative shapes to give a digital identifier. The pattern is adapted to be optically readable by standard imaging equipment at the same time as the primary alignment mark is imaged, requiring no major equipment modification and only minimal modification to image analysis. The recognition key is preferably laid down by the same process as the primary  
25 mark, for example employing photolithographic techniques. However, the pattern making up the recognition key is designed to be optically imaged for recognition purposes only, and not for determination of alignment differences. The structure can accordingly be made from structural element(s) which optimise this aspect, and might therefore be substantially larger than the  
30 structures making up the primary alignment mark.



The recognition key pattern comprises a small number of pattern areas, for example between four and eight, in each of which areas a marking may be present or absent, the pattern of such markings thus providing the unique  
5 identification. In particular, in each pattern area a marking is either substantially entirely present or substantially entirely absent. The arrangement of which pattern areas are present and which are absent gives the unique key. For example, for simplicity it might be preferable if a mark is absent in a single pattern area.

10

Preferably, the recognition key pattern has a generally square or rectangular outline. This is particularly the case where the corresponding primary mark has generally square or rectangular symmetry. In particular, the horizontal and vertical directions of such a square or rectangular outline correspond to  
15 the horizontal and vertical directions of a similarly square or rectangular overlay mark, and in use with the x and y directions of symmetry in the optical imaging apparatus. As a consequence of this geometry, each pattern area is similarly preferably square or rectangular. The recognition key pattern then preferably comprises a linear or two-dimensional array of such pattern areas,  
20 for example consisting of between one and four such areas in each of a row and column direction, corresponding in use to the x and y directions in the optical imaging apparatus.

Each pattern area preferably has dimensions of between 1 and 4  $\mu\text{m}$ , and  
25 particularly preferably comprises a 1  $\mu\text{m}$  square. All pattern areas making up the recognition key pattern are preferably identically sized and shaped.

In particular, the key pattern comprises a square or rectangular area subdivided into a two dimensional array of square or rectangular pattern areas.

This gives a highly readable identification mark, maintaining the square or rectangular symmetry of many of the alignment marks with which it is intended to be used, and accordingly easily readable by the imaging equipment. Suitable overall pattern dimensions are from 2 to 8  $\mu\text{m}$ , allowing  
5 pattern area dimensions of 1 to 2  $\mu\text{m}$  for ease of imaging. In particular pattern areas are 1 to 2  $\mu\text{m}$  squares.

In a particular embodiment the recognition key pattern comprises a square divided into four equal sub-square pattern areas as above described. Each sub-  
10 square pattern area is either present or absent in the recognition key pattern. Mostly preferably, the recognition key pattern comprises a generally L-shaped mark, wherein there are four such sub-square pattern areas in one of which a mark absent. The mark provides four distinct patterns (dependent upon the orientation of the L-shape) which are easily readable and distinguished. This  
15 is sufficient for many purposes.

It is well known that optimal performance depends on measurement being centred on the optic axis of the imaging device. Overlay marks are usually symmetric about this centre, with the overlay error being the measured  
20 displacement of the centres. Conveniently, to avoid introducing asymmetry, the recognition key may be located at the centre. Alternatively, a plurality of recognition keys are provided away from the centre.

The advantages of existing target designs are retained. The measurements are  
25 made from a single image so that speed of measurement is not compromised. The measurement is made using an optical image, so that existing imaging tools can be used. Overlay error may be quantified using any suitable known or specifically developed image processing technique.

Thus, in accordance with the present invention in a second aspect a method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of:

- 5 laying down a first mark portion in association with a first layer;  
and laying down a second mark portion in association with a second layer;  
the first and second mark portions being so structured as to together constitute,  
when the mark is properly aligned, at least one pair of test zones, each test  
zone comprising a first mark section formed as part of the first mark portion  
10 and a second mark section formed as part of the second mark portion each  
comprising a plurality of elongate rectangular mark structures in parallel array  
adjacently disposed to form the said test zone test zone such that the mark  
structures in each test zone are in alignment within the test zone, said  
alignment being in a first direction in half of the test zones and in a second  
15 direction substantially at 90° thereto in the other test zones, and wherein the  
test zones making up the or each pair are laterally displaced relative to each  
other along one of the said directions.

Similarly, in accordance with the present invention in a third aspect a method  
20 for determining the relative position between two or more layers of an  
integrated circuit structure comprises the steps of:

- laying down a first mark portion in association with a first layer, and laying  
down a second mark portion in association with a second layer, the first and  
second mark portions being so structured as to together constitute at least one  
25 pair of test zones as hereinabove described;  
optically imaging the two test zones in the said first and second directions;  
collecting and digitizing the image;  
numerically analysing the digitized data to obtain a quantified measurement of  
the misalignment of the first and second mark portions.

It is important to emphasise that each mark portion making up the overlay metrology mark is laid down in direct association with the associated layer, and in particular is preferably developed within or on the surface of the said layer. For example each mark portion is printed on the said layer. Each mark  
5 portion is preferably laid down by a photolithographic process.

In a preferred embodiment of the method of the invention, the overlay metrology mark incorporates an identification mark serving as a recognition key as hereinbefore described. The method thus comprises, in association with  
10 the step of laying down of an alignment mark portion associated with a second layer, and for example contemporaneously therewith, laying down in association with the said mark portion an identification portion comprising a simple optically readable mark divided into a small number of pattern areas in each of which areas a marking may be present or absent, the  
15 pattern of such markings providing a unique identification key so as to serve to identify the alignment mark portion.

Optical imaging of the mark is preferably carried out using imaging microscopy, and for example bright field microscopy. Other preferred features  
20 of the methods will be understood by analogy with the foregoing.

The invention will now be described by way of example only with reference to Figures 1 to 6 of the accompanying drawings, wherein:

25 Figures 1 to 3 are general schematics of an overlay metrology mark in accordance with three embodiments of the invention;

Figure 4 is a plan view of a suitable identification recognition key for use in accordance with a preferred embodiment of the invention;

Figure 5 illustrates use of the key of figure 4 in association with the mark of figure 3;

Figure 6 illustrates example substructures for a mark structure for use with a  
5 mark in accordance with the invention.

The overlay metrology mark comprises a first or reference mark portion on a first lower layer and a second or alignment mark portion on a second layer above the first layer, for example an uppermost layer. Where complete marks  
10 are illustrated in the figures, the second mark portion is represented by darker grey-shaded structures. The first mark portion, configured to be at least partially visible in conjunction with the second, is represented by lighter grey-shaded structures.

15 The invention lies in the arrangement of test structures in a repeating array. The structures and any sub-structures making up the test structures are formed using any suitable processes. Typically these will include lithographic processes that are generally known in the art. Misalignment is measured using imaging systems and image analysis techniques, which may be standard  
20 systems and techniques that are generally known in the art or systems and techniques modified to be optimized specific to the marks in accordance with the invention.

Figure 1 illustrates a top plan view of an alignment mark according to one  
25 embodiment of the invention. The mark is shown in the intended configuration that results when the tested layers of a structure are in proper alignment. The mark consists of two mark portions, one on each layer, so serving as overlay and reference.

In figure 1 there are two test zones. Each zone has an overall square shape. The zones are spaced along the dotted line equidistantly about the dot so that each square zone is located mirror-symmetrically on the dotted line. In use this is an X or Y mirror direction of the bright field imaging microscope or  
5 other device, with the dot being the optic centre.

In this implementation, four groups of linear mark structures are shown. The lines in the first two groups are oriented vertically making up the first zone, while the lines in the final two groups are oriented horizontally. The pairs of  
10 lines are designed to be printed exactly side by side. The overlay measurement is the relative displacement of one set of lines from the other, which may conveniently be measured using any standard or specially modified technique and analysis.

15 To optimise differentiation between reference and overlay the line pitch is arranged to be significantly larger than process tolerance limits for overlay error. The pitch of the lines is also arranged to match the resolution of the imaging microscope. In the example the line pitch is constant, giving the array a constant periodicity. Line pitch is conveniently broadly equal to line width,  
20 both being around 1  $\mu\text{m}$  in the illustrated implementation.

Figure 2 illustrates a top plan view of an alignment mark according to one embodiment of the invention. The mark is shown in the intended configuration that results when the tested layers of a structure are in proper  
25 alignment. The mark consists of two mark portions, one on each layer, so serving as overlay and reference.

In figure 2 there are four test zones. Each zone has an overall square shape as in figure 1. The zones are identical in size and spaced along the dotted lines

equidistantly in pairs about a common centre. In use these are X and Y mirror directions of the bright field imaging microscope or other device, with the intersection of the lines being the optic centre.

5 Again each zone consists of an array of lines from the overlay and an array from the reference. The lines in two of the zones are oriented vertically, while the lines in the final two zones are oriented horizontally. The pairs of lines in each zone are designed to be printed exactly side by side. This produces a cross pattern similar to that of traditional targets, but with each zone  
10 symmetrically on the axes whilst retaining a square geometry. This design meets the goals of separation of the target lines from each layer in order to avoid interaction between the images, axial symmetry and offers more image detail than other designs. The use of isolated groups of lines for each layer also permits application of novel image analysis techniques.

15

Figure 3 illustrates a top plan view of an alignment mark representing a minor variant of figure 2. Again, there are four zones of similar line arrays, but the orientation within equivalent zones is varied. This is intended to illustrate that provided zones are present to give both X and Y measurement, it is not critical  
20 whether the linear structures making up the two zones in each pair share an orientation or are in opposite orientation.

Figure 4a shows a basic recognition key suitable for use with the overlay metrology mark of the invention in accordance with a preferred embodiment  
25 thereof. The mark is shown in top plan view. Increasingly, new measurement structures do not provide an easy pattern recognition target as there is no isolated well-resolved image in the resist. The key comprises a specific mark printed in the resist layer. The mark consists of a 2  $\mu\text{m}$  square mark area subdivided into a two by two array of 1  $\mu\text{m}$  square pattern areas. Three of  
30 these are covered by the mark material and one absent. The effect is to

produce a key comprising a 2  $\mu\text{m}$  square from which one corner is omitted, giving a general L-shape.

Any corner may be omitted, allowing four unique pattern recognition targets to be created as illustrated in figure 4b. The simplicity of the design makes this easy to image, and easy to distinguish between the four targets, so that the key provides a clear digital identifier of a given overlay mark with which it is associated, and greatly assists in ensuring the correct overlay mark is imaged. Overlay targets can be positioned nearby but will be safe from pattern recognition error if the keys are different. The probability of locating the wrong target can be reduced by varying the omitted corner in adjacent targets, increasing the distance to a potentially confusing pattern recognition key.

Figure 5 illustrates use of the key of figure 4 in association with the marks of figure 3. A key is placed centrally within a mark and further keys laid down at the corners. This example is illustrative only of the various arrangements that could be envisaged.

Figure 6 illustrates example substructures for a mark structure for use with a mark in accordance with the invention. A single individual test structure from those making up each array of a mark in accordance with the invention is shown to the left, being an elongate rectangular structure. Such an individual test structure may optionally be made using design rule sized sub-structures to address issues of process induced inaccuracy, as is well known. In the illustrated three examples on the right, the rectangular structure comprises an array of sub-resolution features (lines, dots or squares etc.) to form the required shape. Because the small features are not resolved, they are not individually visible through the microscope, giving the appearance of a single contiguous structure. The mark-space ratio of the sub-resolution features can be adjusted to meet the optimal performance criteria of the printing process.



Claims

1. An overlay metrology mark for determining the relative position between  
5 two or more layers of an integrated circuit structure comprising a first  
mark portion associated with a first layer and a second mark portion  
associated with a second layer, wherein the first and second mark  
portions together constitute, when the mark is properly aligned, at least  
10 one pair of test zones, each test zone comprising a first mark section  
formed as part of the first mark portion and a second mark section  
formed as part of the second mark portion each comprising a plurality of  
elongate rectangular mark structures in parallel array adjacently disposed  
to form the said test zone such that the mark structures in each test zone  
15 are in alignment in a first direction within the test zone but are  
substantially at 90° with respect to the mark structures of at least one  
other test zone in alignment in a second direction, and wherein the test  
zones making up the or each pair are laterally displaced relative to each  
other along one of the said directions.
- 20 2. An overlay metrology mark in accordance with any preceding claim  
wherein each pair of zones are laterally disposed relative to each other  
such as in use to have mirror symmetry about an imaging axis of the  
imaging apparatus.
- 25 3. An overlay metrology mark in accordance with claim 1 wherein each  
mark portion is developed within or on the said layer.
4. An overlay metrology mark in accordance with claim 2 wherein each  
mark portion is printed on the said layer by a microlithographic process.

5. An overlay metrology mark in accordance with any preceding claim wherein each test zone has a generally square or rectangular outline shape, the rectangular directions corresponding to the said first and second directions and to the mirror axes of the imaging equipment in use.  
5
6. An overlay metrology mark in accordance with claim 5 wherein test zones are generally square.
7. An overlay metrology mark in accordance with any preceding claim  
10 wherein only two test zones are present, and wherein the first and second mark sections of the first zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the first mark portion and the second mark portion, the first and second mark sections of the second zone comprise similar arrays but disposed at right  
15 angles thereto, and the two test zones are laterally spaced along a line which is parallel to the direction of the test structures in one zone, and perpendicular to the direction of the test structures in the other zone.
8. An overlay metrology mark in accordance with one of claims 1 to 6  
20 comprising more than one pair of test zones, wherein each pair is laterally disposed equidistantly about a common centre in one or other of the said two directions.
9. An overlay metrology mark in accordance with claim 8 comprising a  
25 single such pair disposed in a first direction and a single such pair in a second direction.
10. An overlay metrology mark in accordance with claim 9 wherein the first  
30 and second mark sections of each zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the

first mark portion and the second mark portion, and wherein the first and second mark sections of two zones are in the first direction and the first and second mark sections of the other two zones in similar arrays but disposed at right angles thereto, and the two test zones in each pair are laterally spaced in respectively an X and Y direction about common centres.

11. An overlay metrology mark in accordance with any preceding claim wherein the elongate rectangular mark structures comprise single monolithic rectangular structures.

12. An overlay metrology mark in accordance with any one of claims 1 to 10 wherein the elongate rectangular mark structures comprise arrangements of substructures constituting together a general elongate rectangular outline.

13. An overlay metrology mark in accordance with claim 12 wherein the elongate rectangular mark structures comprises a row or column as the case may be of smaller constituent test structures, for example a row or column of squares.

14. An overlay metrology mark in accordance with any preceding claim wherein each elongate rectangular test structure and/or each constituent test structure comprise arrangements of design rule sized sub-structures.

15. An overlay metrology mark in accordance with claim 14 wherein the arrangements of design rule sized sub-structures are selected from parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array,

arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns.

16. An overlay metrology mark in accordance with any preceding claim  
5 wherein the pitch of the elongate rectangular structures is of constant period in each mark section.
17. An overlay metrology mark in accordance with claim 16 wherein the  
period is identical in all mark sections.
- 10 18. An overlay metrology mark in accordance with claim 16 or 17 wherein all rectangular test structures in a test zone, and preferably in the whole mark, have identical widths and spacing.
- 15 19. An overlay metrology mark in accordance with any preceding claim wherein each test structure has a width of around 0.5 to 2  $\mu\text{m}$ , and wherein spacing between test structures in the array is between  $\frac{1}{2}$  and two structure widths.
- 20 20. An overlay metrology mark in accordance with any preceding claim wherein each mark section comprises at least five test structures in each direction.
- 25 21. A method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of:  
laying down a first mark portion in association with a first layer;  
and laying down a second mark portion in association with a second layer;

the first and second mark portions being so structured as to together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone such that the mark structures in each test zone are in alignment within the test zone, said alignment being in a first direction in half of the test zones and in a second direction substantially at 90° thereto in the other test zones, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions.

22. A method for determining the relative position between two or more layers of an integrated circuit structure:  
laying down a first mark portion in association with a first layer, and laying down a second mark portion in association with a second, the first and second mark portions being so structured as to together constitute at least one pair of test zones as hereinabove described;  
optically imaging the two test zones in the said first and second directions;  
collecting and digitizing the image;  
numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

23. The method of claim 22 wherein optical imaging of the mark is carried out using bright field microscopy.

24. The method of one of claims 21 to 23 wherein each mark portion is developed within or on the said layer.

25. The method of one of claims 21 to 24 wherein each mark portion is laid down by a microlithographic process.
- 5 26. A mark or method substantially as hereinbefore described with reference to the accompanying drawings.

Figure 1

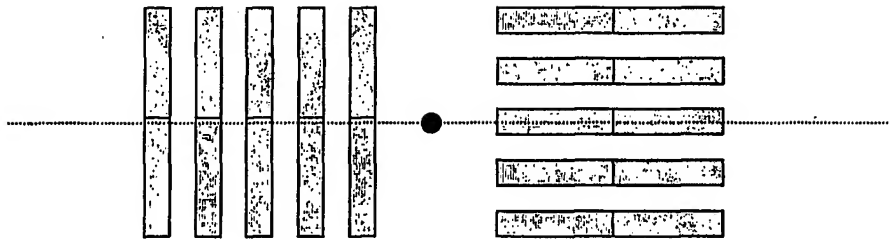


Figure 2

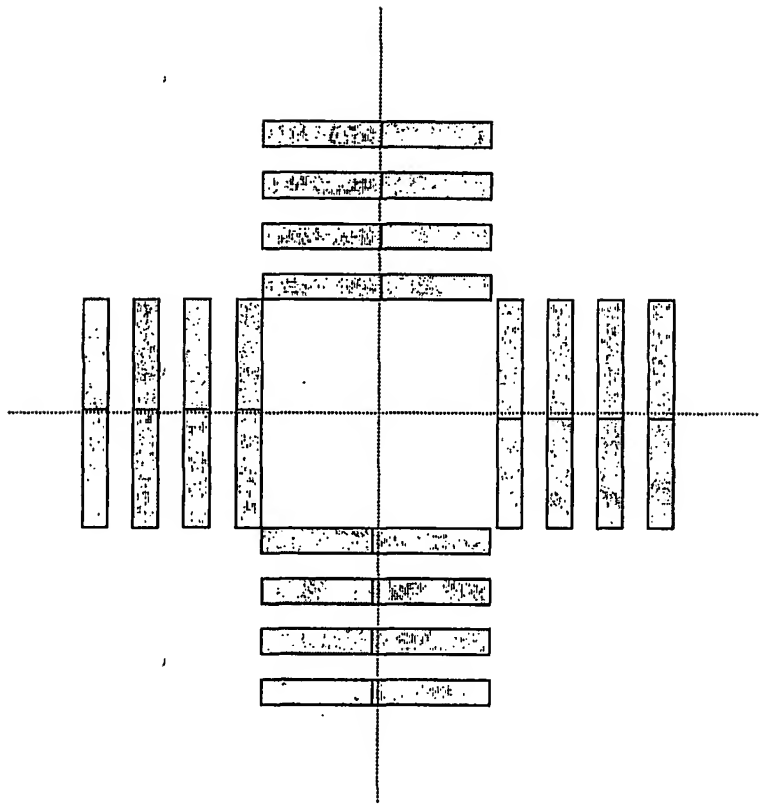
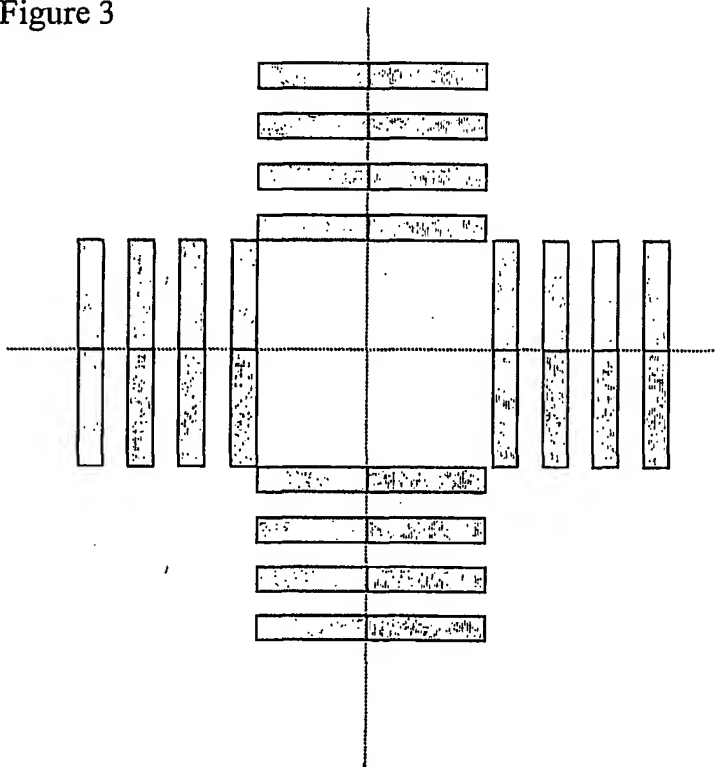


Figure 3





3/4

Figure 4a

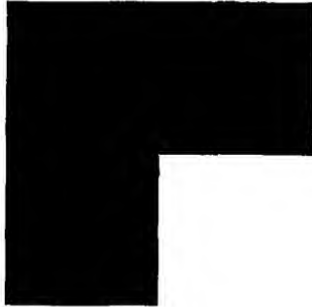
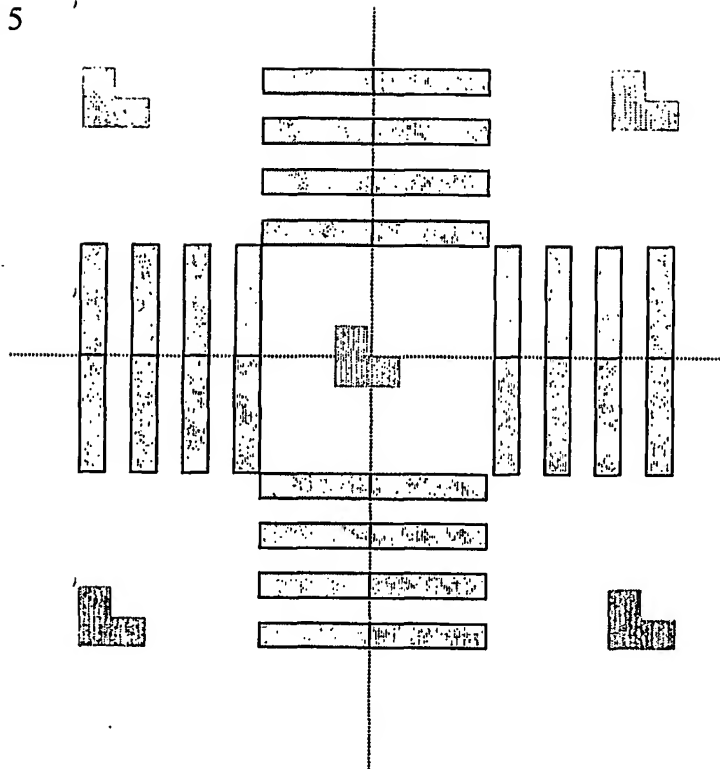


Figure 4b



Figure 5



4/4

Figure 6

